I. THE CLAIMS DEFINE ALLOWABLE SUBJECT MATTER

The Office Action rejects claim 1 under 35 U.S.C. §103(a) as unpatentable over U.S. Patent No. 6,320,568 to Zavracky ("Zavracky") in view of U.S. Patent No. 6,104,367 to McKnight ("McKnight") and U.S. Patent No. 5,646,644 to Furuhashi et al. ("Furuhashi"); claims 2, 6, 7 and 17 under 35 U.S.C. §103(a) as unpatentable over Zavracky, McKnight, Furuhashi and further in view of U.S. Patent No. 6,489,956 to Deering ("Deering"); claim 3 under 35 U.S.C. §103(a) as unpatentable over Zavracky, McKnight, Furuhashi, Deering and further in view of U.S. Patent No. 6,326,642 to Yamazaki et al. ("Yamazaki"); claim 4 under 35 U.S.C. §103(a) as unpatentable over Zavracky, McKnight, Furuhashi, Deering, and further in view of U.S. Patent No. 6,498,617 to Ishida et al. ("Ishida"); claim 5 under 35 U.S.C. §103(a) as unpatentable over Zavracky, McKnight, Furuhashi, Deering, and further in view of U.S. Patent No. 6,333,766 to Kougami et al. ("Kougami"); claim 9 under 35 U.S.C. §103(a) as unpatentable over Zavracky, McKnight, Furuhashi, Deering and further in view of U.S. Patent No. 5, 973,456 to Osada et al. ("Osada"); claim 18 under 35 U.S.C. §103(a) as unpatentable over Zavracky, McKnight, Furuhashi, Deering and further in view of U.S. re-issued Patent No. RE37,879 E to Takeuchi ("Takeuchi"); claim 14 under 35 U.S.C. §103(a) as unpatentable over Zavracky, McKnight, Furuhashi, Deering and further in view of U.S. Patent No. 6,462,722 to Kimura et al. ("Kimura"); and claims 19, 24 and 28 under 35 U.S.C. §103(a) as unpatentable over Zavracky in view of U.S. Patent No. 4,156,927 to McElroy et al. ("McElroy"), U.S. Patent No. 6,104,641 to Itou ("Itou"), U.S. Patent No. 6,278,428 to Smith et al. ("Smith") and U.S. Patent No. 5,841,411 to Francis ("Francis"). These rejections are respectfully traversed.

The applied art does not disclose a display device including, "a storing section that stores a data signal to control display, the storing section having a memory cell configured by a static circuit," as recited in independent claim 1.

Instead, McKnight discloses that "while old pixel data values are being held or stored on the pixel electrode 681, a new pixel data value is loaded into the pixel circuit or cell by applying a high row select signal on row select wire 687 and concurrently applying the pixel data value on data wire 686." The FET 685 passes the pixel data value, which is preferably an analogue pixel data value, through to the gate of the FET 684.

Additionally, the Office Action admits that Zavracky does not teach a storing section that stores a digital data signal to control display, but asserts that McKnight makes up for this deficiency. However, as noted above, McKnight discloses that while old pixel data values are being held or stored in the pixel electrode 681 (with the pole down signal 688 being kept low such that the FET 683 is off) a new pixel data value is loaded into the pixel circuit or cell by applying a high row select signal on row select wire 687 and concurrently applying the pixel data value on data wire 686.

Additionally, Furuhashi does not disclose a storing section that stores a data signal to control display, the storing section having a memory cell configured by a static circuit. Accordingly, none of the applied art teaches or suggests each feature of independent claim 1.

The applied art does not disclose a display device, including "a storing section storing a data signal when a write signal is transmitted through a respective one of the plurality of write lines," as recited in independent claim 2.

As discussed above with respect to claim 1, Zavracky, McKnight, and Furuhashi do not disclose this claimed feature. Moreover, Deering does not make-up for the deficiencies of Zavracky, McKnight and Furuhashi. Accordingly, none of the applied art teach or suggest each feature of independent claim 2.

With respect to the rejection of claim 4, Ishida should be removed as prior art in the present application under any subsection of 35 U.S.C. §103. On April 22, 2002, Applicant filed a Corrected Claim for Priority and Certified Copy of Japanese Patent Application No.

2000-09-3576 which was filed in Japan on March 30, 2000. The U.S. filing date of Ishida is October 13, 2000, which is after the priority date to which this application is entitled. Accordingly, Applicant respectfully submits that Ishida should not be considered as prior art in the present application under any subsection of 35 U.S.C. §103.

None of the applied art discloses a display device including, "a storing section having at least one memory cell configured by a static circuit, the storing section storing a data signal when a write signal is transmitted through a respective one of the plurality of write lines," as recited in independent claim 14.

As discussed above with respect to claim 2, Zavracky, McKnight, Furuhashi and Deering do not disclose this claimed feature. Moreover, Kimura does not make-up for the deficiencies of Zavracky, McKnight, Furuhashi and Deering.

The applied art does not disclose a display device including, "a storing section having at least one memory cell configured by a static circuit, the storing section storing a data signal when a write signal is transmitted through a respective one of the plurality of write lines," as recited in independent claim 17.

For the same reasons as discussed above with respect to claim 2, Applicant respectfully asserts that none of the applied art teach or suggest each feature of independent claim 17.

None of the applied art discloses a display device including, "each of the plurality of dots including a storing section having a memory cell configured by a static memory, the storing section storing a data signal supplied through a respective one of the plurality of data lines, each of the plurality of dots including an electro-optical conversion section that performs an electro-optical conversion on the basis of the data signal held by the storing section," as recited in claim 19.

For the same reasons as discussed above, Applicant respectfully asserts that none of the applied art teach or suggest each feature of independent claim 19.

Additionally, a write signal (or a scanning signal) in an ordinary display device is usually supplied to write signal lines in serial order from the first write signal line irrespective of rewriting. In contrast, it is unnecessary to supply a write signal to write signal lines in the claimed display device. Instead, the write signal only has to be supplied to a dot to be written. Accordingly, none of the applied art teach or suggest each feature of claim 19.

The applied art does not disclose a display device, including, "each of the plurality of dots including an electro-optical conversion section that performs an electro-optical conversion on bases of a data signal supplied through a respective one of the plurality of data lines," as recited in independent claim 28.

The Office Action asserts that a timing controller section and a memory controller section are integrally formed on a substrate according to Smith, col. 7, lines 40-42. However, Smith discloses only "a controlled unit coordinates the above-described activities of the display panels and display panel interface." Accordingly, Applicant respectfully asserts that new claim 28 is allowable.

For the same reasons as discussed above, Applicant respectfully asserts that new independent claims 29 and 34 are also allowable.

Furthermore, Applicant respectfully submits that the Office Action has pieced together multiple references to teach the claimed invention. However, MPEP §2143.01 instructs that "[t]he mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F. 2d 680, 16 USPQ 2d 1430 (Fed. Cir. 1990)." MPEP §2143.01 further instructs that "[a]lthough a prior art device 'may be capable of being modified to run the way the apparatus is claimed, there must be a suggestion or motivation in

the reference to do so.'" Applicant respectfully submits that the references do not provide such a suggestion or motivation.

Applicant respectfully submits that the only motivation to piece together the multiple references of the Office Action is found in the Applicant's own application. MPEP §2141 instructs that "the references must be viewed without the benefit of impermissible hind sight vision afforded by the claimed invention." MPEP §2143 instructs that "the teaching or suggestion to make the claimed combination and the reasonable expectation of success must be found in the prior art, not the Applicant's disclosure. *In re Vaeck*, 947 f.2d 488, 20, USPQ 1438 (Fed. Cir. 1991)." The Federal Circuit has clearly held that "the motivation to combine references cannot come from the invention itself." *Heidelberger Druckmaschinen AG v. Hantscho Commercial Products, Inc.*, 21 f.3d 1068, 30 USPQ 2d 1377 (Fed. Cir. 1993).

Thus, Applicant respectfully submits that the Office Action has not established a *prima facie* case of obviousness and that the rejections under 35 U.S.C. §103(a) should be withdrawn.

Furthermore, the claimed invention provides numerous advantages as found on pages 28-32 of the present application.

For at least these reasons, it is respectfully submitted that independent claims 1, 2, 14, 17, 19, 28, 29 and 34 are distinguishable over the applied art. The remainder of the claims that depend from independent claims 1, 2, 14, 19 and 34 are likewise distinguishable over the applied art for at least the reasons discussed above, as well as for the additional features they recite.

II. CONCLUSION

For at least these reasons, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1-35 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in better condition for allowance, the Examiner is invited to contact Applicant's undersigned representative at the telephone number listed below.

Respectfully submitted,

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JAO:JML/vgp

Attachments:
Appendix
Amendment Transmittal

Date: May 5, 2003

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
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APPENDIX

Changes to Claims:

The following is a marked-up version of the amended claims:

1. (Twice Amended) A display device, comprising:

~~at least one of a semiconductor and an insulating substrate~~ a plurality of write lines;

a plurality of data lines;

a plurality of dots disposed correspondingly to intersections between the plurality of write lines and the plurality of data lines, each of the plurality of dots that is a minimum unit for displaying, including:

a storing section that stores a~~digital~~ data signal to control display, the storing section having a memory cell configured by a static circuit; and

a display control section that performs display control on the basis of the digital data signal ~~stored by said storing section~~ held by the storing section~~;~~

~~the storing section and display section being provided in each dot which is a minimum unit of display and being arranged on the at least one of a semiconductor and an insulating substrate~~.

2. (Twice Amended) A display device, comprising:

~~at least one of a semiconductor and an insulating substrate~~ a plurality of write lines;

a plurality of data lines;

~~a storing section configured by at least one storing circuit provided at each of interconnections of~~ a plurality of dots disposed correspondingly to intersections between the plurality of write lines and ~~a~~the plurality of data lines, each of the plurality of dots that is a

minimum unit for displaying ~~correspondingly to an array pattern of a dot as a minimum unit of display so that~~, including:

a storing section storing a data signal when a write signal is transmitted through ~~said write line and an image signal as a digital data signal to control display is transmitted through said data line, the image signal is stored~~ a respective one of the plurality of write lines;

a converting section that converts a value based on a value of the ~~image signal stored by said~~data signal held by the storing section into an analog signal; and

a display control section that performs tonal control ~~using a liquid crystal~~ on the basis of ~~an~~the analog signal converted by ~~said~~the converting section~~;~~

~~the storage section and display section being provided in each dot which is a minimum unit of display and being arranged on the at least one of a semiconductor and an insulating substrate~~.

3. (Twice Amended) The display device ~~as claimed in~~ according to claim 2, ~~said~~ the at least one storing circuit ~~of said storing section being~~ including a memory cell configured by a static circuit.

4. (Thrice Amended) The display device ~~as claimed in~~ according to claim 2, ~~said converting section pulse-width-modulating the value based on the image signal to convert the value into~~ the analog signal being represented as a PWM waveform generated by the converting section.

5. (Thrice Amended) The display device ~~as claimed in~~ according to claim 2, ~~said~~the converting section converting the ~~value based on the image~~data signal ~~into~~ to the analog signal ~~modulated to a pulse width based on a~~including γ-characteristic.

14. (Twice Amended) A display device, comprising:

~~at least one of a semiconductor and an insulating substrate~~a plurality of write lines;

a plurality of data lines;

a ~~storing section configured by at least one storing circuit provided at each of interconnections of a~~plurality of dots disposed correspondingly to intersections between the plurality of write lines and ~~a~~the plurality of data lines, each of the plurality of dots that is a minimum unit for displaying ~~correspondingly to an array pattern of a dot as a minimum unit of display so that~~, including:

a storing section having at least one memory cell configured by a static circuit, the storing section storing a data signal when a write signal is transmitted through ~~said write line and an image signal as a digital data signal to control display is transmitted through said data line, the image signal is stored~~ a respective one of the plurality of write lines;

~~at least one active device provided respectively connected to said storing circuits of said storing section and current-driven luminescent devices having areas corresponding to place values represented by image signals stored in said storing circuits; and~~

a luminescent section including a plurality of luminescent elements having different areas; and

~~a display control section provided in each dot to control emission of light of said current-driven luminescent devices on the basis of the values of the image signals stored in said storing circuits,~~an active device section connected to the storing section and the ~~display control section being arranged on the at least one of a semiconductor and an insulating substrate~~ luminescent section.

15. (Thrice Amended) The display device ~~as claimed in~~ according to claim ~~13~~ 14, ~~said current-driven~~ the plurality of luminescent ~~devices~~ elements being ~~structured by~~ EL ~~devices~~elements.

16. (Thrice Amended) The display device ~~as claimed in~~ according to ~~claim 13~~ 14, ~~said current driven~~ the plurality of luminescent ~~devices~~ elements being ~~structured by~~ organic EL ~~devices~~ elements.

17. (Twice Amended) A display device, comprising:

~~at least one of a semiconductor and an insulating substrate~~ a plurality of write lines;

a plurality of data lines; and

a ~~storing section configured by at least one storing circuit provided at each of interconnections of a~~plurality of dots disposed correspondingly to intersections between the plurality of write lines and a~~data lines, each of the~~ plurality of ~~data lines correspondingly to an array pattern of a dot as~~dots being a minimum unit of displaying ~~display so that~~, and including:

a storing section having at least one memory cell configured by a static circuit, the storing section storing a data signal when a write signal is transmitted through ~~said write line and an image signal as a digital data signal to control display is transmitted through said data line, the image signal is stored~~ a respective one of the plurality of write lines; and

~~at least one active device provided respectively connected to said storing circuits of said storing section and liquid crystal driving sections having areas corresponding to place values represented by image signals stored in said storing circuits; and~~

~~a display control section provided in each dot to perform tonal control using a liquid crystal on the basis of the values of the image signals stored in said storing circuits, and the storing section and the display control section being arranged on the at least one of a semiconductor and an insulating substrate~~

an active device section connected to the storing section.

18. (Thrice Amended) The display device ~~as claimed in~~ according to ~~claim 2~~ 1, further including a plurality of read lines ~~laid~~ disposed correspondingly to ~~said dot array pattern so that~~ the plurality of dots, ~~if~~ read out of the data signal held by the storing section being performed when a read signal is transmitted, ~~the image signals stored in said storing circuits are read out of said storing section~~ through a respective one of the plurality of read lines.

19. (Twice Amended) A display device, comprising:

~~at least one of a semiconductor and an insulating substrate~~ a plurality of write lines;

a plurality of data lines;

~~a display drive~~ an active-matrix section having a plurality of ~~word lines, a~~ dots disposed correspondingly to intersections of the plurality of write lines and ~~a~~ the plurality of data lines ~~laid correspondingly to an array pattern of a dot as a minimum unit of display, and a display control section operating, when at least a write signal is transmitted through said write lines and the image signals are transmitted through said data lines, on the basis of said storing section that stores the image signals, the image signals and a word signal transmitted through said word lines, provided in each of the dot array patterns~~, each of the plurality of dots including a storing section having a memory cell configured by a static memory, the storing section storing a data signal supplied through a respective one of the plurality of data lines, each of the plurality of dots including and electro-optical conversion section that performs an electro-optical conversion on the basis of the data signal held by the storing section;

~~a word line driver section that controls transmission of a word signal to said word lines;~~

a column decoder section that selects a data line of the plurality of data lines; and

a row decoder section that selects a row ~~for transmitting a write signal to said write lines, to transmit the write signal to a selected row;~~ of the plurality of write lines through which a write signal is transmitted, the write signal being supplied to only a dot to be written of the plurality of dots

~~a column decoder section that selects said data line;~~

~~a column selection switch section that transmits the image signals as data signals to control display to said data line selected by said column decoder section;~~

~~the sections being integrated and integrally formed on the at least one of a semiconductor and an insulating substrate~~.

20. (Twice Amended) The display device ~~as claimed in~~ according to claim 19, each of the plurality of dots further including a converting section that converts a value based on ~~the image signals stored in said storing section into an analog signal provided in each dot array pattern in said display drive section, and said display control section operates on the basis of the analog signal and the word signal~~ a value of the data signal held by the storing section into an analog signal.

21. (Twice Amended) The display device ~~as claimed in~~ according to claim 19, ~~said word lines being laid to transmit the word signal to said display control section on~~ further comprising a plurality of first lines for supplying a voltage as a power source to the storing section, the plurality of first lines being shared between two rows of the plurality of write signal lines.

22. (Thrice Amended) The display device ~~as claimed in~~ according to claim 19, ~~said word line driver section and said row decoder section being allocated correspondingly to a length of said display drive~~ the row decoder section being allocated correspondingly to a

length the active-matrix section in a column direction, and ~~said~~ the column decoder section ~~and said column selection switch section~~ being allocated correspondingly to a length of ~~said display drive~~ the active-matrix section in a row direction.

23. (Twice Amended) The display device ~~as claimed in~~ according to claim 19, ~~each~~ further including a column selection switch ~~structuring said column selection switch section being allocated correspondingly to a width of said dot array pattern~~ section that transmits the data signal to a data line of the plurality of data lines selected by the column decoder section.

24. (Thrice Amended) The display device ~~as claimed in~~ according to claim 19, ~~said~~ the row decoder ~~section selecting~~ that selects a row ~~for transmitting the~~ of the plurality of write lines through which a write signal is transmitted on the basis of an address signal ~~representing a storage position~~.

25. (Twice Amended) The display device ~~as claimed in~~ according to claim ~~23~~ 19, ~~said~~ the column decoder section ~~selecting said~~ that selects a data line of the plurality of data lines on the basis of ~~the~~ an address signal.

26. (Twice Amended) The display device ~~as claimed in~~ according to claim ~~25~~ 19, further including:

a plurality of pixels each of which being provided by three dots ~~that develop and display in red, blue and green as light source colors being provided as one pixel, the image signals being input on a one-pixel unit basis, and~~ for red, green and blue, respectively, of the plurality of dots;

~~said~~ the column decoder section selecting data lines ~~to store the image signals in an amount of one pixel~~ of the plurality of data lines corresponding to a respective pixel of the plurality of pixels; and

the data signal being supplied together to the three dots included in a respective one of the plurality of pixels.

27. (Twice Amended) The display device ~~as claimed in~~ according to claim ~~25~~ 19, ~~three dots that develop and display in red, blue and green as light source colors being provided as one pixel, the image signals being input on a plural-pixel-unit basis, and~~ further including:

a plurality of pixels each of which being provided by three dots for red, green and blue, respectively, of the plurality of dots;

~~said~~ the column decoder section selecting data lines ~~to store the image signals in an amount of a~~ of the plurality of data lines corresponding to respective pixels of the plurality of pixels; and

the data signal being supplied together to the three dots included in the respective pixels.

28. (Twice Amended) ~~The~~ A display device ~~as claimed in claim 19, further including~~ comprising:

a substrate;

a plurality of write lines;

a plurality of data lines;

an active-matrix section having a plurality of dots disposed correspondingly to intersections of the plurality of write lines and the plurality of data lines, each of the plurality of dots including an electro-optical conversion section that performs an electro-optical conversion on basis of a data signal supplied through a respective one of the plurality of data lines;

a column decoder section that selects a data line of the plurality of data lines; and

a row decoder section that selects a row of the plurality of write lines through which a write signal is transmitted;

a timing controller section that controls at least timing of transmitting ~~the~~ an address signal on the basis of which at least one of the column decoder section and the decoder section selects at least one data line of the plurality of data lines and the row of the plurality of write lines; and

~~a memory controller section that controls transmission of the image signals;~~ the plurality of write lines, the plurality of data lines, the active-matrix section, the column decoder section, the row decoder section, and the timing controller section ~~and the memory controller section~~ being ~~integrated and~~ integrally formed on ~~said at least one of a semiconductor and an insulating~~ the substrate.